PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 3 :		(11) International Publication Number: WO 83/ 03916
G09G 1/28	A1	(43) International Publication Date: 10 November 1983 (10.11.83)

(21) International Application Number: PCT/GB83/00119

(22) International Filing Date: 22 April 1983 (22.04.83)

(31) Priority Application Number: 8211723

(32) Priority Date: 22 April 1982 (22.04.82)

(33) Priority Country: GB

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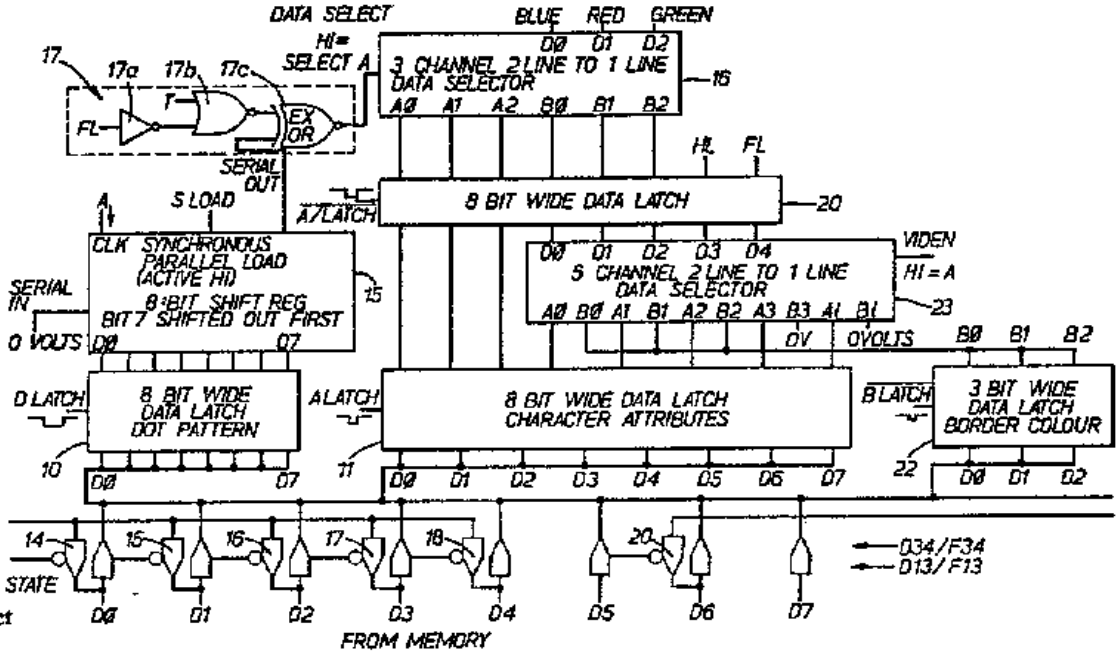
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB, GB (European patent), JP, LU (European patent), NL (European patent), SE (European patent), US.

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: DISPLAY FOR A COMPUTER



(57) Abstract

A coloured display for a computer is derived using a first set of digital words representing locations in a pixel matrix for the pattern to be displayed and a second set of digital words representing foreground and background colours for the pattern on the basis of a conventional character display whereby to reduce the amount of storage required for the colour information while permitting high resolution graphics. Circuits are provided for converting digital R, G, B signals into analogue Y, U, V signals and each of these circuits comprises a control transistor in whose collector circuit is connected the base of an output transistor and in whose emitter circuit are connected parallel switches and resistances which switches are controlled by signals derived from the digital R, G, B signals whereby to alter the base bias of the output transistor.

DISPLAY FOR A COMPUTER

The present invention relates to computers and more particularly to coloured displays for computers.

Coloured displays for computers are already well known but most conventional displays require large amounts of memory for producing high resolution graphics in colour as well as complex circuitry.

From one aspect, an object of the present invention to reduce the amount of memory required in order to provide high resolution graphics in colour.

Preferably, this is achieved by considering the display as a matrix of dots in order to provide the graphics and by grouping a multiplicity of dots together for colour purposes. This enable a reduction in the amount of information which is required to be stored and hence a reduction in the amount of storage required.

The advantage of this proposal is that the graphics is highly defined whereas the colour information is less highly defined as is usually the case for most displays.

From another aspect, an object of the present invention is to provide less complex circuitry for deriving the conventional U,V,Y signals which are used for PAL television receivers.

Preferably, the circuitry is incorporated into the peripheral cells of an uncommitted logic array (ULA).

Features and advantages of the present invention will

become apparent from the following description given by way of example when taken in conjunction with the accompanying drawings, in which:-

Figure 1 shows a block circuit diagram of part of the circuit for generating high resolution graphics in colour;

Figure 2 shows a circuit for generating one of the colour difference signals for the PAL system of television;

Figure 3 shows a circuit for generating the other colour difference signal for the PAL system of television;

Figure 4 shows a circuit for generating the luminance signal for the PAL system of television; and

Figure 5 shows a detailed circuit diagram of the arrangement shown in Figure 1 and for producing the signals used for the circuits shown in Figures 2, 3 and 4.

Before described the invention, it is considered helpful if a general discussion of the graphics is given first. Conventionally a VDU read out for a computer cosnsits of a "page" of characters on the screen of the VDU arranged in rows and columns. For the sake of the present discussion it is assumed that there are 24 rows with 32 character locations in each row of the display. It is also assumed that the size of each character position is such that 8 raster scan lines are required to fully display one row of the display. With this arrangement, it is apparent that not all the active area of the television screen is utilised by the display but this is not considered to be a disadvantage due to the fact that the display can be generated for either a 525 line television system or a 625 line television system.

The character locations of the display can be used to display either alpha-numeric symbols or graphical symbols but it will be appreciated that when displaying graphical symbols, the display will be somewhat crude due to the small number of character locations. It has already

been proposed to sub-divide the character locations for graphics display using, what are termed "pixels" and it is this latter concept which we are using. In our case, we envisage notionally dividing up the display area into a matrix of pixels of 192 rows each containing 256 pixels.

When displaying a matrix of pixels in black and white, the amount of memory required is manageable but as soon as one wishes to display in colour, the amount of memory required increases considerably if each pixel is to have it own individual colour.

We have now produced an arrangement whereby the background colours are treated in the "old" manner as if the display were still displaying character positions whereas the foreground colour is displayed as a pixel plane display with a consequent considerable saving in the amount of memory required. In other words each character location requires 8 bytes of data to define the dot pattern i.e. the pixel pattern in the character location but only 1 byte of data, the attribute byte, for the colour of the character location. Each attribute byte comprises a number of bits representing the foreground colour, a number of bits representing the background colour and preferably a bit to indicate whether or not to cause the character location to flash and also preferably a further bit to allow two different levels of illumination to cause particular desired areas to be highlighted. The number of bits required for the colour information is chosen having regard to the size of the byte and the number of colours which it is wished to use. In the present case, eight colours are used which means that 3 bits are required for backgroud colour and 3 bits for foreground colour giving an 8 bit attribute byte. Thus, a high resolution graphics display can be produced in colour using a memory device, preferably a random access memory of the dynamic type. The size of the memory device

is a function of the number of pixels and also the number of attribute bytes. With our system of 192 x 256 pixels and 768 character locations, the memory device has to be capable of storing approximately 6k bytes of data for the 192 x 256 pixel pattern plus approximately ¾k of data for the attribute bytes for the 768 character locations.

As mentioned above, each character location consists of eight pixels horizontally by eight rows i.e. TV raster scan lines vertically. In order to generate the raster scan TV picture, the memory device has to be accessed sequentially in a cycle that repeats every TV field. For every eight pixels generated, the computer needs two bytes of data from memory, a pixel pattern byte and an attribute byte. These two bytes are loaded into respective intermediate registers from which they then are loaded into further registers. The six least significant bits of the attribute byte represent the foreground and background colours. A data selector is controlled by the pixel pattern bytes shifted out of their register to select foreground or background colour for each pixel and fed to a colour generator circuit for generating a 3 bit (R.G.B) signal for each pixel.

The operation of the memory and registers will now be described in more detail with reference to Figure 1. Eight bit data words (bytes) are fed from memory (not shown) to eight input pins DØ to D7. The eight bit words are fed in parallel to the inputs of an intermediate pixel pattern latch 10 and an attribute latch 11. The latch 10 or the latch 11 is gated by the processor depending on whether the data to be loaded into the latch is pixel pattern data or colour (attribute) data. For each raster scan line, the memory is addressed to sequentially recover the 32 pixel pattern bytes for the 256 pixels for that line. With each of these bytes, a further portion of memory is addressed in order to recover the attribute

byte for eight pixels associated therewith.

The data in the latch 10 is then transferred to a further latch 15. The bits of data held in the latch 15 are shifted out serially. Each bit represents a pixel and the logical level of each bit determines whether it is a foreground or a background pixel. Each bit as it is shifted out is used to gate a 3-channel 2 line to 1 line selector 16 via a logic circuit 17 which will be described in more detail later. The result is a 3-bit R,G, or B signal.

Attribute data held in latch 11 is likewise transferred to a further latch 20. It will be recalled that 6 bits of the 8 bit data word represent foreground and background colours. These six bits are fed to the data selector 16. The remaining two bits are control bits one for indicating the level of brightness of the display for that pixel, this being indicated by the output labelled HL and the other for indicating whether or not flashing of the pixel is required, this being indicated by the output labelled FL. Flashing, in this case, is achieved by causing the pixel in question to alternately display the foreground and background colour at a rate determined by a clock signal T. Thus, the logic circuit 17 contains an inverter 17a for inverting the signal on the output F1 and feeding the inverted signal as an input an OR gate 17b to whose input clock signal T is applied. The output of the date 17b is fed as one input to an EX-OR gate 17c whose other input is the data bit indicating a foreground pixel.

In operation if a data bit representing a foreground pixel is shifted out of the latch 15 to one input to the EZ-OR gate 17c, the data selector 16 is conditioned to cause the 3 bits of attribute data indicative of a foreground colour to be fed to the Blue, Red and Green outputs of the selector. If flashing is required, a

signal is cyclically applied to the other input of the EX-OR gate 17c to cause its output to alternate which in turn causes the output from the data selector to alternate the foreground and background colours.

It will be noted that a further latch 22 and data selector 23 are present. These are used so that the colour of the picture area around the pixel display area on the television screen can be defined to have a different colour to that of the background of the pixel display area.

This process is repeated along a raster line with 32 pixel pattern bytes being successively fed to the latch 10 while the 32 associated attribute bytes are fed to the latch 11. For the next line, a fresh set of 32 pixel pattern bytes are transferred successively from memory to the latch 10 but the associated attribute bytes are the same as the previous line. This process is repeated line by line until 8 lines have been displayed. Thereafter a fresh set of attribute bytes are used for the next 8 lines.

Although the output of the data selector 16 is an indication of the colour required, it is not in a form which can be utilised by the colour circuits of a conventional television receiver and so further processing of the R.G.B output from the data selector 16 is required. A further aspect of the present invention lies in the circuitry used to process the R,G,B signals into the more conventional Y,U,V signals.

Attention is directed now to Figure 2 which shows a circuit for deriving the U signal for a colour television receiver. The digital R,G,B outputs from the data selector 16 are combined with sync, blank and burst signals to provide correct phase digital signals in a digital to analogue converter circuit which is shown in Figure 2. It will be seen that the R,G,B signals are now Blue"

$\overline{\text{Green}}$" and $\overline{\text{Red}}$" and are used to gate a respective transistor switch 31, 32, 33 to cause varying amounts of base bias to be applied to an output transistor 34. The $\overline{\text{Burst}}$ signal is also used to gate a transistor 36 which also varies the amount of base bias on transistor 34. This is achieved by all the Blue", $\overline{\text{Green}}$", $\overline{\text{Red}}$" and $\overline{\text{Burst}}$ circuits being connected between the emitter of a control transistor 35 and ground thus varying the current through the control transistor when it is switched on as a function of whether one or more of the switches controlled by the Blue", $\overline{\text{Green}}$", $\overline{\text{Red}}$" and $\overline{\text{Burst}}$ is operated.

Figure 3 shows a circuit similar to Figure 2 but for the V signal. Equivalent parts to Figure 2 are increased by ten in Figure 3 and further description will be omitted except to say that in this case the R,G,B signals are combined with the sync, blank and burst signals to form Red*, $\overline{\text{Green*}}$, $\overline{\text{Blue*}}$, $\overline{\text{Burst*}}$ and Burst* input signals to transistors 43, 42, 41, 46 and 48 respectivley.

Figure 4 shows the luminance digital to analogue converter circuit which in addition ot the Red', Green', Blue' and $\overline{\text{Sync}}$ signals derived from the output of the data selector 16 has a further input $\overline{\text{HL}}$ which is derived from the highlight data bit in the attribute bytes.

As with the circuits in Figures 2 and 3, Red', Green' and Blue' signals are used to gate transistors 53, 52, 51 respectively which are in the emitter circuit of a control transistor 55. The $\overline{\text{HL}}$ signal is used to gate a transistor 56 which affects the base current to the control transistor 55. The $\overline{\text{sync}}$ signal gates a further transistor 57 which is used to directly control the base bias of the output transistor 54.

Detailed description of the circuit shown in Figures 2, 3 and 4 is omitted since resistance values are given

on the drawings and it is considered that in view of this, the operation is apparent to one skilled in the art.

The circuits shown in Figures 2, 3 and 4 have been designed for their simplicity and also so that they can be incorporated as peripheral circuits of an uncommitted logic array (ULA) which can be used to provide the reaminder of the colour and pixel matrix display circuit.

For completeness, Figure 5 which is made up of Figures 5A, 5B, 5C and 5D shows a detailed circuit diagram showing in detail the construction of the blocks shown in Figure 1 as well as the circuits for producing the correct phase R,G,B signals used in Figures 2, 3 and 4. Where appropriate the blocks are shown in Figure 5 in broken lines and given the same reference numeral as in Figure 1. The circuits shown in Figures 2, 3 and 4 are contained in the block 60 in Figure 5D.

CLAIMS:

1. Apparatus for producing a coloured display from a computer, comprising memory means having a first portion of a capacity capable of storing a multiplicity of digital words each constituted by a plurality of binary digits and representing a pattern to be displayed, and a second portion of a capacity smaller than the capacity of the first section for storing a multiplicity of further digital words each constituted by a further plurality of binary digits and representing the colour of the pattern to be displayed, each of said further digital words being associated with a plurality of the first-mentioned digital words, latch means for receiving one of said first-mentioned digital words and its associated further digital words, and digital colour signal generating means responsive to said first-mentioned and further digital words for producing digital colour signals for a portion of a line of a video raster scan.

2. Apparatus according to claim 1, wherein the latch means includes a first latching arrangement for receiving a first-mentioned digital word and for outputting the binary digits in a serial manner.

3. Apparatus according to claim 2, wherein each of the further digital words includes data representing both foreground and background colour information, and the colour signal generating means includes a 2 channel into 1 data selector responsive to the logical level of each of the binary digits output from the first latching arrangement whereby the colour information representing the foreground or the background information is generated.

4. Apparatus according to claim 1, 2 or 3, and comprising digital to analogue conversion circuitry for producing analogue colour signals from the digital signals output from the digital colour signal generating means.

5. Apparatus according to claim 4, wherein conversion circuitry comprises three digital to analogue conversion circuits, one for generating an analogue signal representing a U signal, one for generating an analogue signal representing a V signal and one for generating an analogue signal representing a Y signal.

6. Apparatus according to claim 5, wherein each of the digital to analogue conversion circuits comprises an output transistor whose base bias is controllable by a control transistor in whose emitter circuit are connected further switching devices responsive to the signals derived from the digital colour signal generating means.

7. A digital to analogue converter circuit for producing an analogue signal representing colour information for a coloured video display, comprising a plurality of switching devices connected in parallel with each other in the emitter circuit of a control transistor whose collector is connected to the base of an output transistor and each responsive to a different one of a plurality of digital signals.

8. A digital to analogue converter circuit according to claim 7, wherein the analogue signal represents a first colour difference signal and comprising a further switching device connected in parallel with said plurality of switching devices and responsive to a further digital signal.

9. A digital to analogue converter circuit according to claim 8, and including a still further switching device connected in parallel with said plurality and further switching devices and responsive to the inverse of the signal applied to the further switching device.

10. A digital to analogue converter circuit according to claim 7 wherein the analogue signal represents a chrominance signal and a synchronising switching device is connected to the base of the output transistor and the collector of the control transistor and responsive to a synchronising digital signal.

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 83/00119

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[3]: G 09 G 1/28

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
IPC[3]	G 09 G

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X,Y	DE, A, 2940322 (SHARP K.K.) 21 August 1980 see page 11, line 19 - page 15, line 15; figure 2 --	1-4,5
Y	US, A, 4303912 (STAFFORD et al.) 1 December 1981 see column 6, line 39 - column 7, line 68; figures 4,5 --	5
A	FR, A, 2083639 (SIEMENS) 17 December 1971 see page 2, line 16 - page 4, line 28; figure 1 ------	6-10

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
10th August 1983	22 SEP. 1983
International Searching Authority [1]	**Signature of Authorized Officer [20]**
EUROPEAN PATENT OFFICE	G.L.M. Kruysenberg

Form PCT/ISA/210 (second sheet) (October 1981)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/GB 83/00119 (SA 5092)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 15/09/83

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
DE-A- 2940322	21/08/80	GB-A-	2044052	08/10/80
		JP-A-	55049738	10/04/80
		US-A-	4310838	12/01/82
		JP-A-	55052503	17/04/80
		JP-A-	55049087	08/04/80
		JP-A-	55092934	14/07/80
US-A- 4303912	01/12/81	None		
FR-A- 2083639	17/12/71	NL-A-	7101932	30/09/71
		DE-A-	2014955	14/10/71

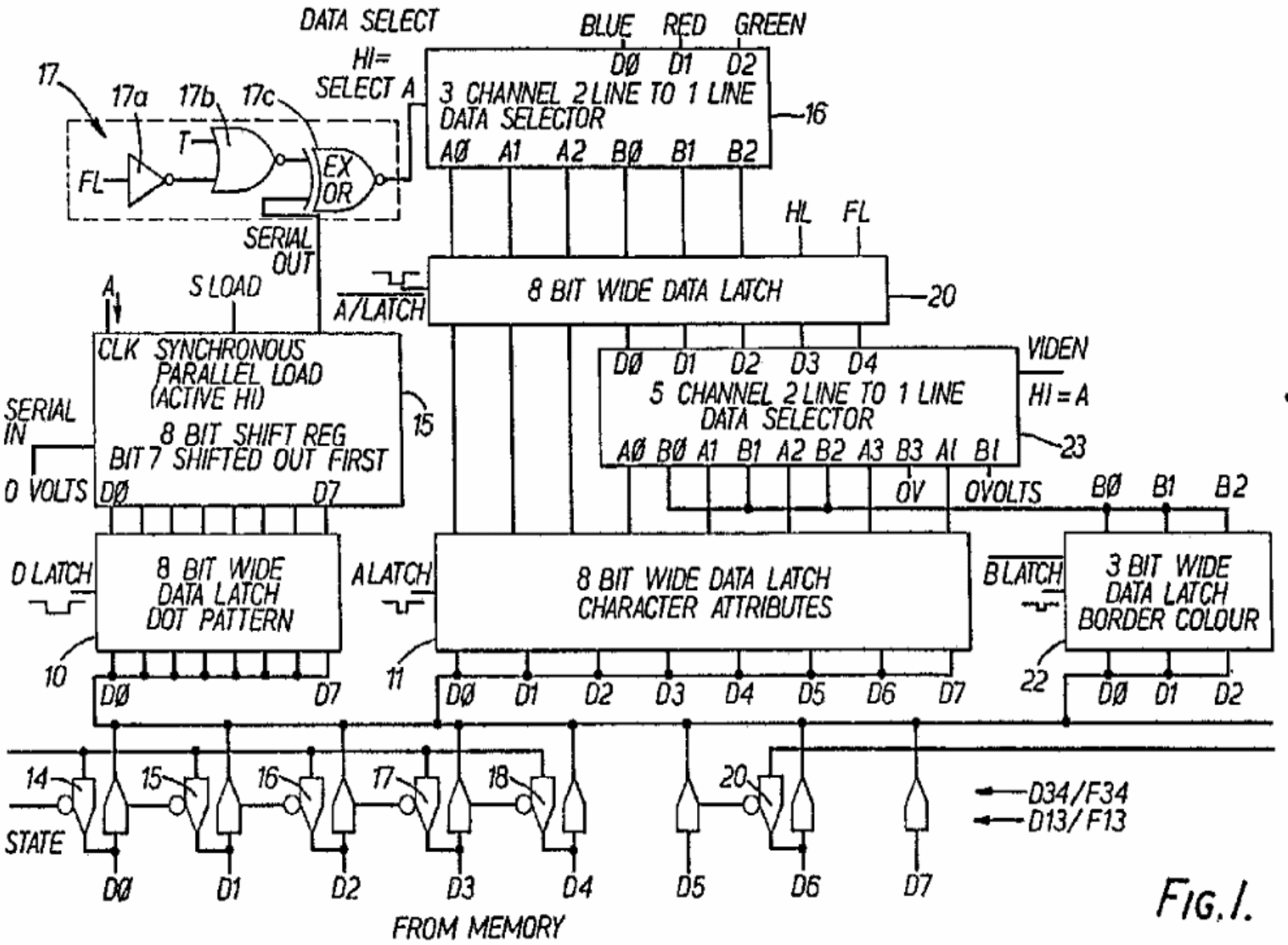

DATA SELECT
HI= SELECT A
BLUE RED GREEN
DØ D1 D2
3 CHANNEL 2 LINE TO 1 LINE DATA SELECTOR
16
AØ A1 A2 BØ B1 B2
17
17a
17b
17c
T
FL
EX OR
SERIAL OUT
HL FL
A
S LOAD
A/LATCH
8 BIT WIDE DATA LATCH
20
CLK SYNCHRONOUS PARALLEL LOAD (ACTIVE HI)
8 BIT SHIFT REG
BIT 7 SHIFTED OUT FIRST
15
SERIAL IN
0 VOLTS
DØ D7
DØ D1 D2 D3 D4
5 CHANNEL 2 LINE TO 1 LINE DATA SELECTOR
AØ BØ A1 B1 A2 B2 A3 B3 A4 B4
23
VIDEN
HI = A
0V
0VOLTS
BØ B1 B2
D LATCH
8 BIT WIDE DATA LATCH DOT PATTERN
10
A LATCH
8 BIT WIDE DATA LATCH CHARACTER ATTRIBUTES
11
B LATCH
3 BIT WIDE DATA LATCH BORDER COLOUR
22
DØ D1 D2 D3 D4 D5 D6 D7
14 15 16 17 18 20
STATE
D34/F34
D13/F13
FROM MEMORY

FIG. 1.

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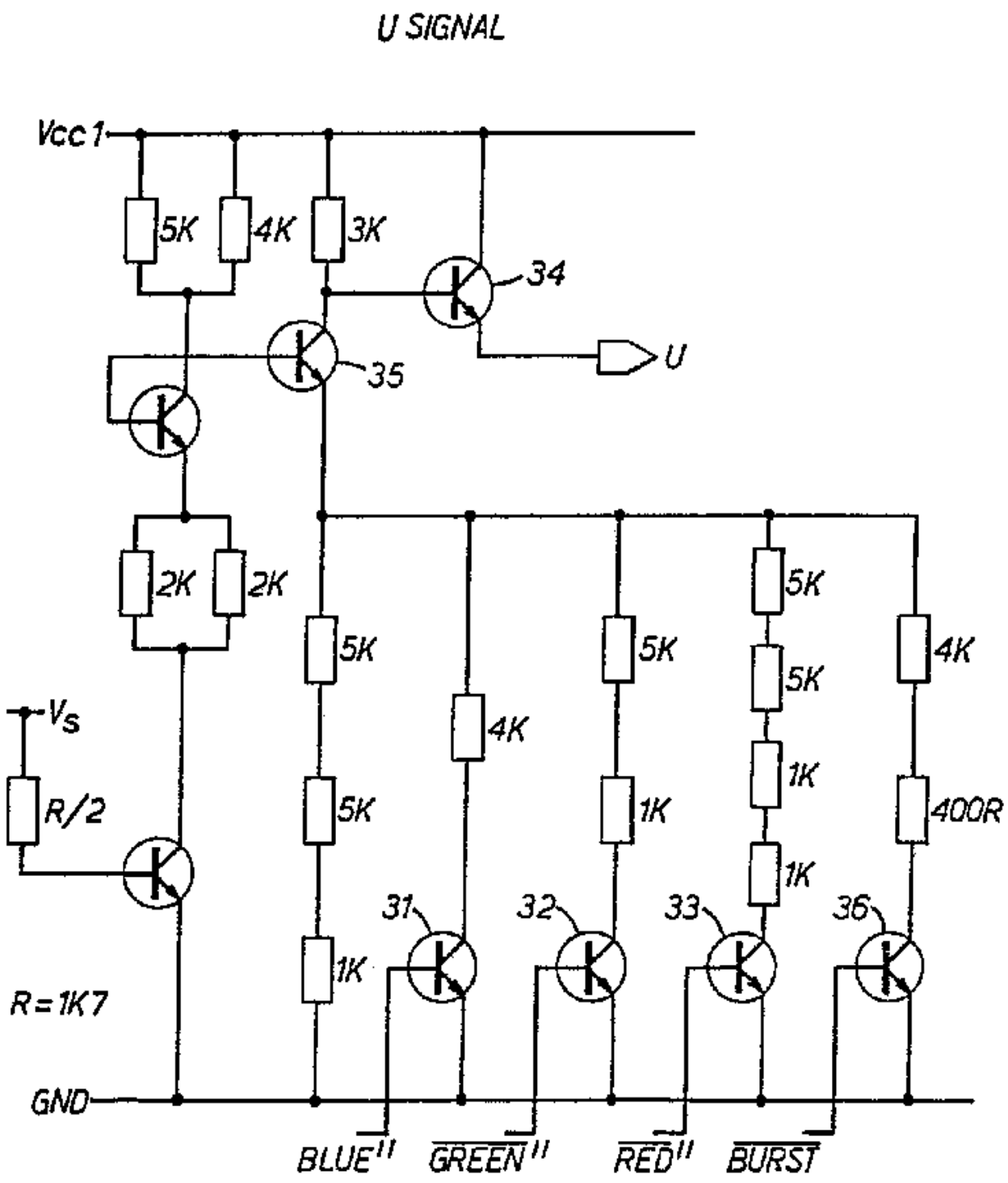
U SIGNAL
Vcc 1
5K
4K
3K
34
35
U
2K
2K
5K
5K
4K
5K
5K
1K
1K
5K
5K
4K
Vs
R/2
400R
31
32
33
36
1K
R=1K7
GND
BLUE''
GREEN''
RED''
BURST

FIG. 2.

3/9

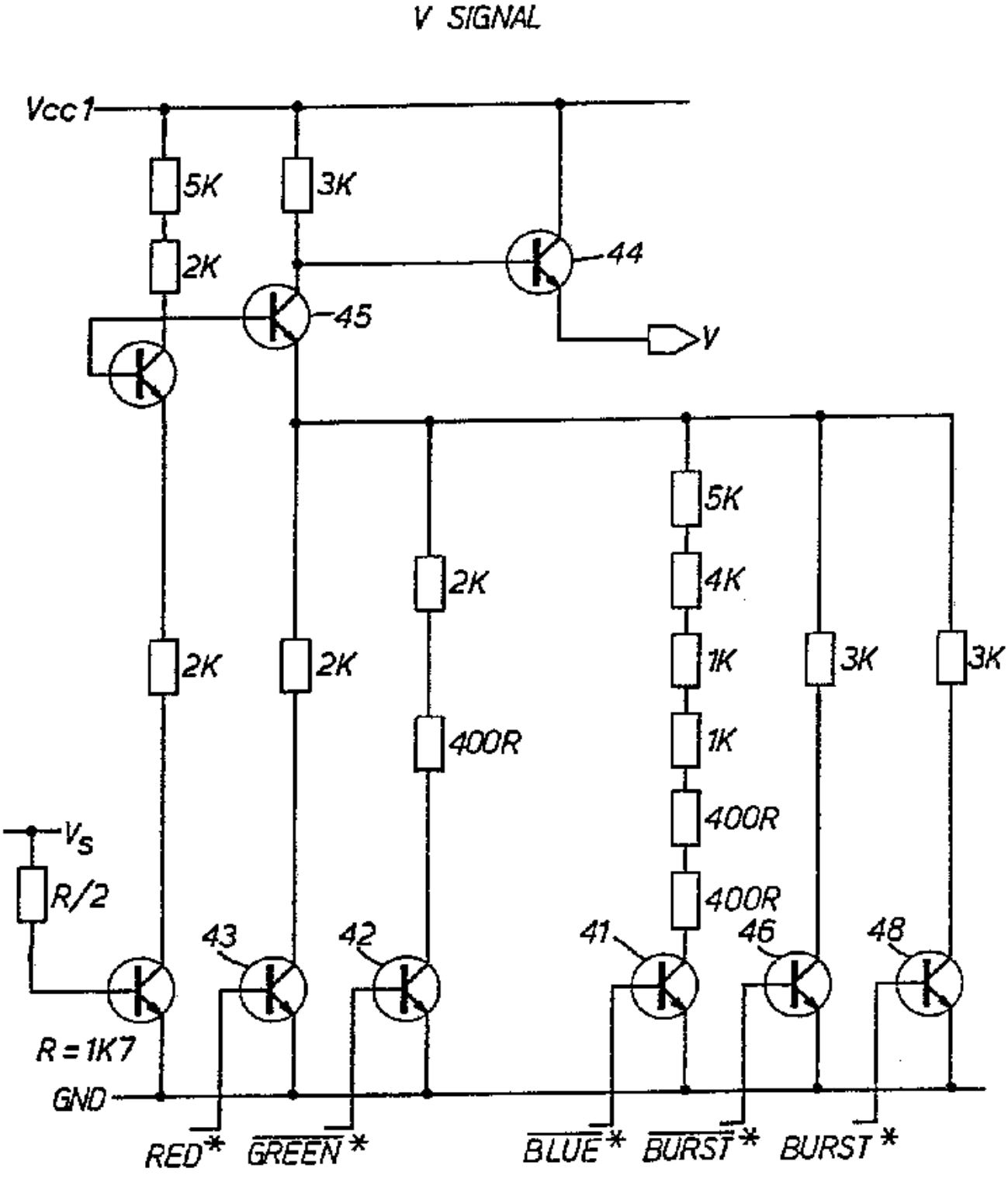
V SIGNAL
Vcc 1
5K
3K
2K
44
45
V
2K
2K
2K
400R
5K
4K
1K
1K
400R
400R
3K
3K
Vs
R/2
R = 1K7
GND
43
42
41
46
48
RED*
GREEN*
BLUE*
BURST*
BURST*

FIG. 3.

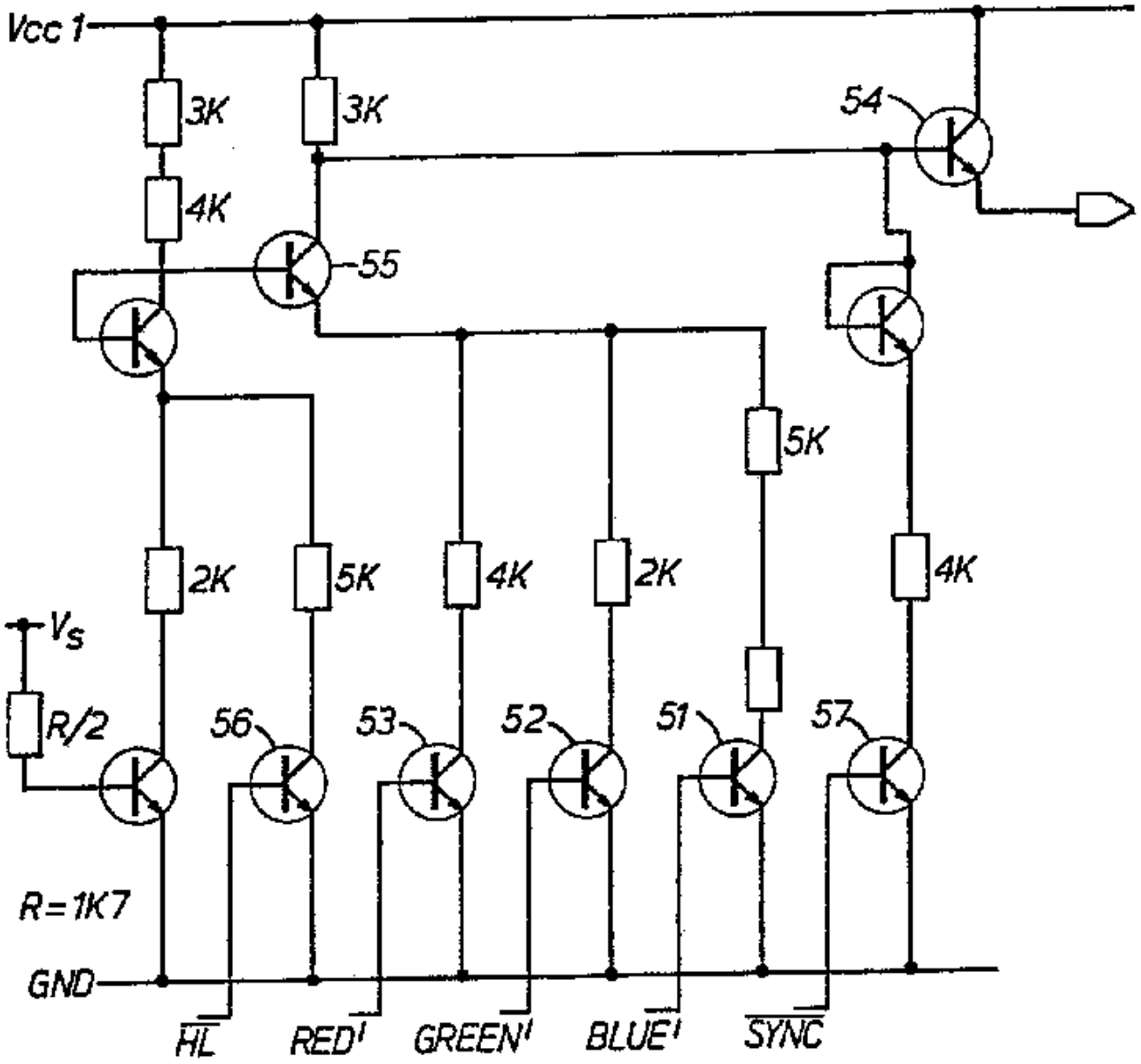
$\overline{Y}$ SIGNAL
Vcc 1
3K
3K
4K
54
55
5K
2K
5K
4K
2K
4K
Vs
R/2
56
53
52
51
57
R=1K7
GND
$\overline{HL}$
RED'
GREEN'
BLUE'
$\overline{SYNC}$

FIG. 4.

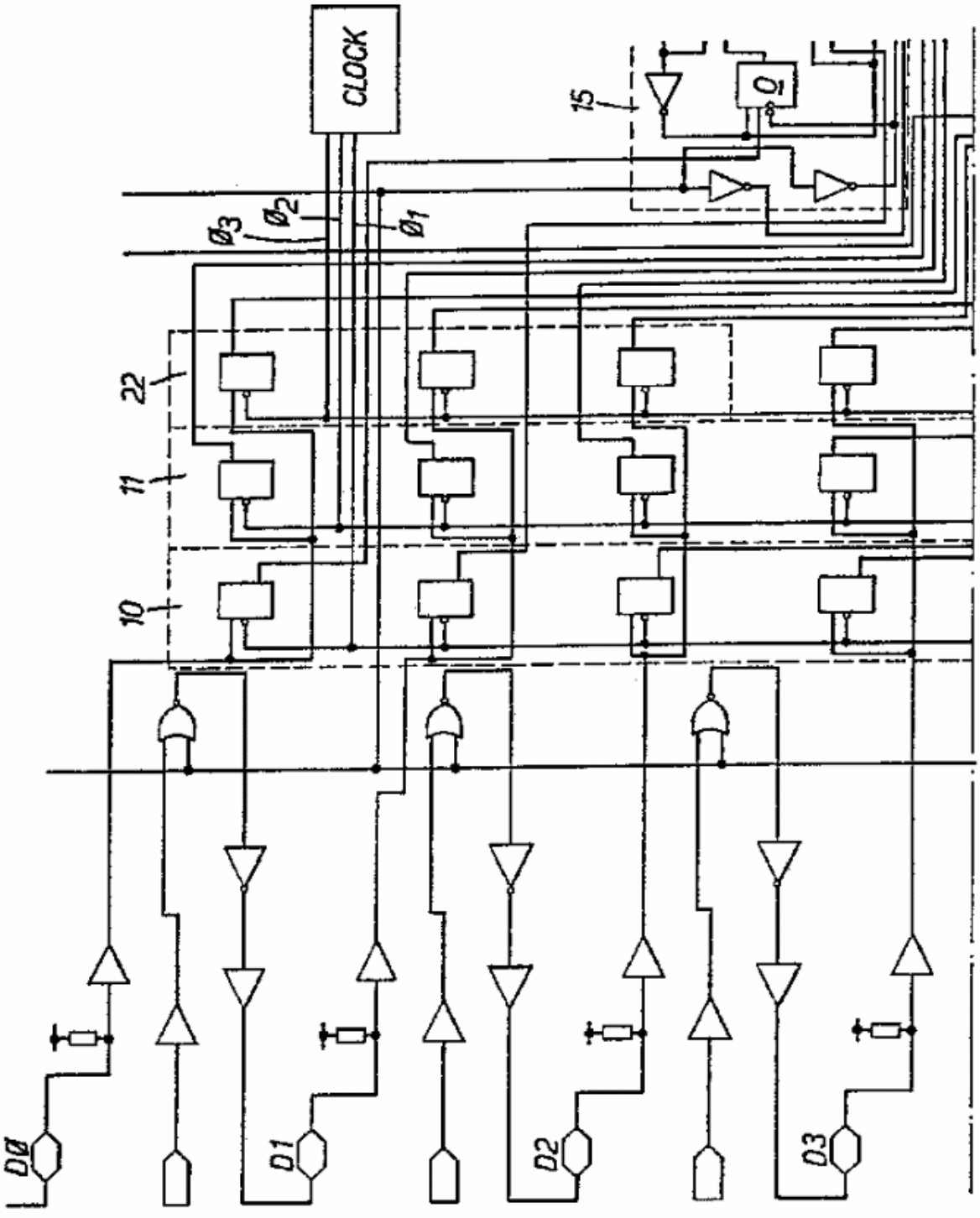

FIG. 5A-1.

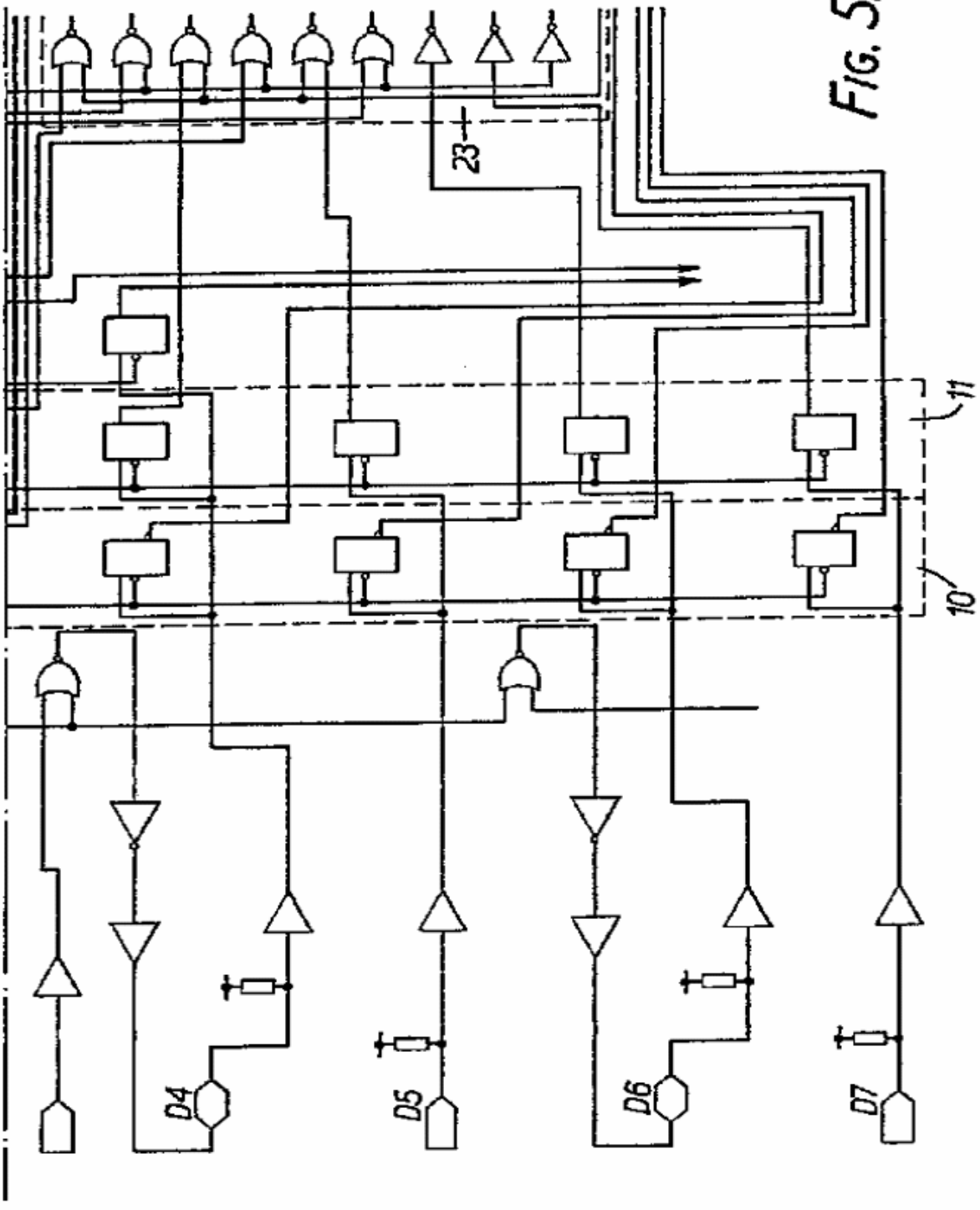

FIG. 5A-2.

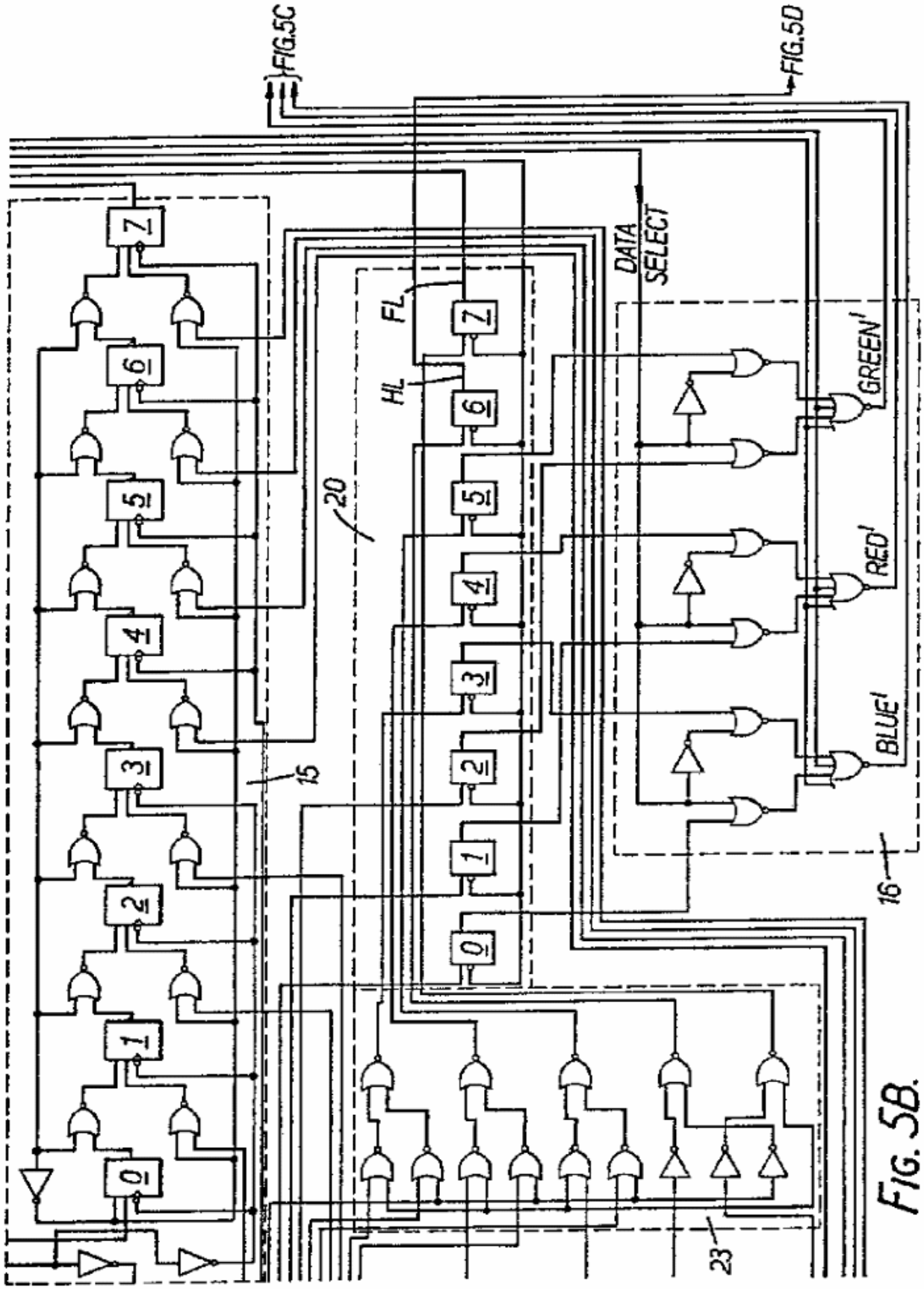
FIG.5C
FIG.5D
DATA SELECT
FL
HL
GREEN'
RED'
BLUE'
20
15
16
23
7
6
5
4
3
2
1
0

FIG. 5B.

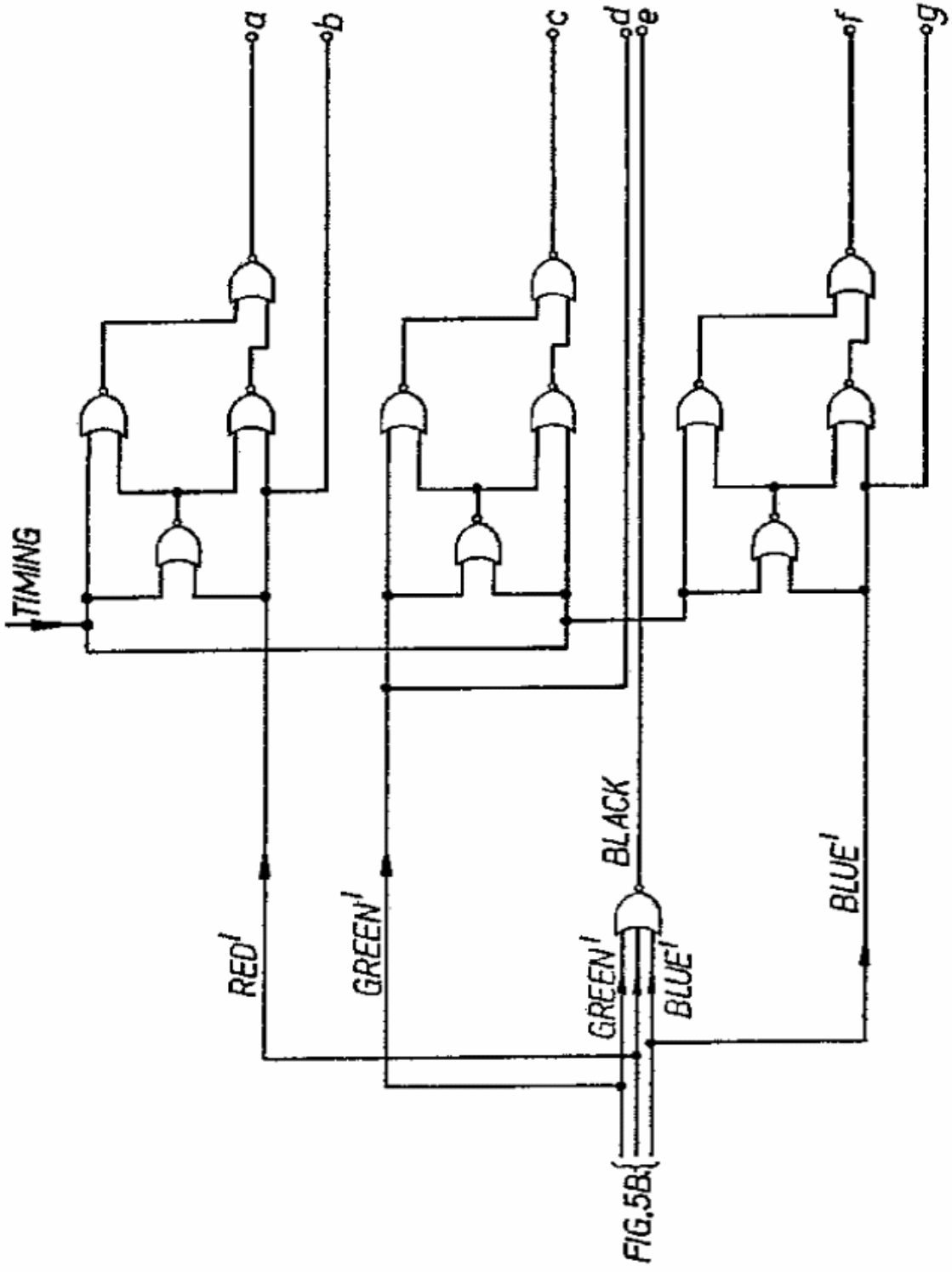

FIG. 5C.

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FIG. 5D.

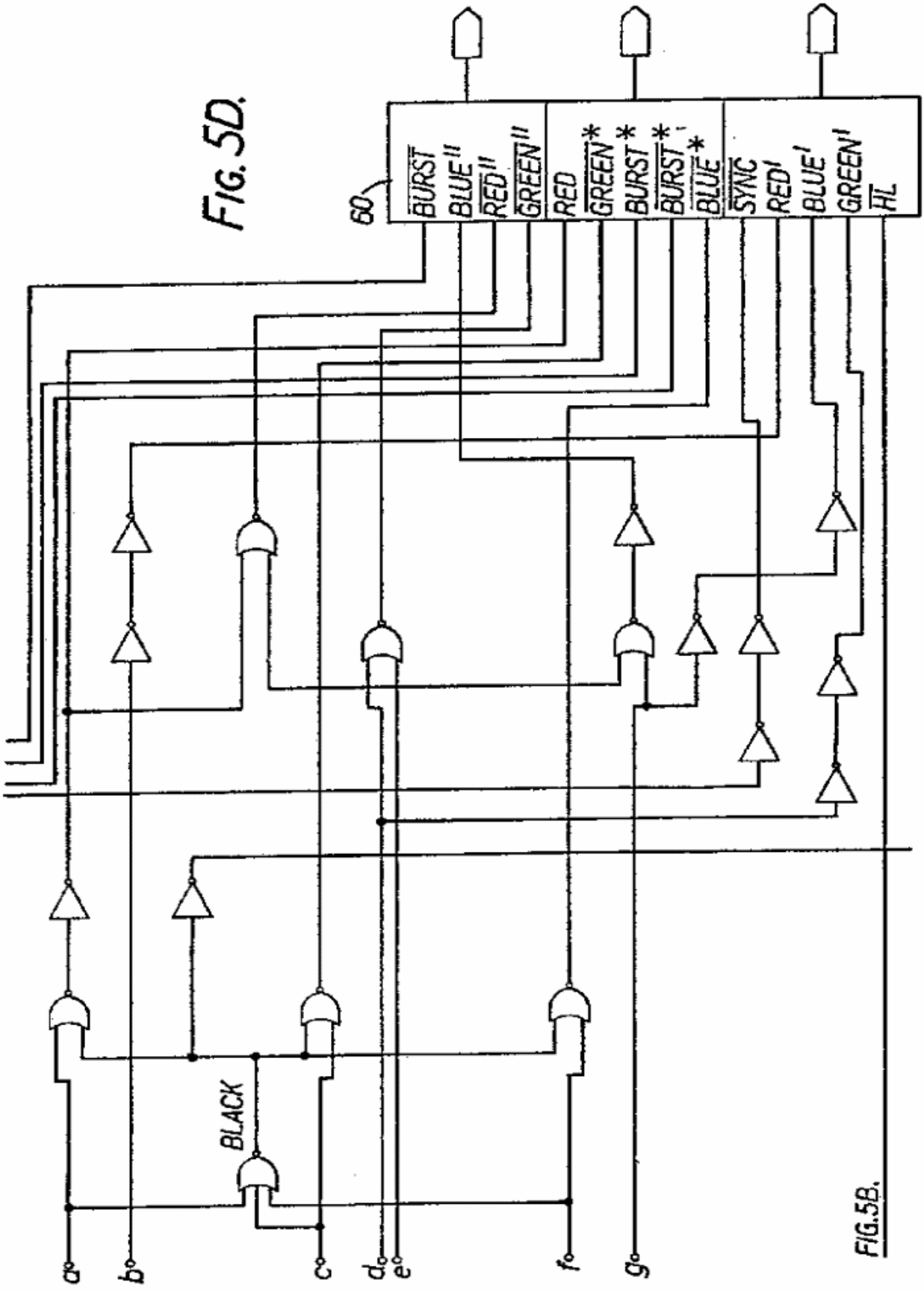

FIG. 5B.

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(72) Inventor; and
(75) Inventor/Applicant *(for US only)* : ALTWASSER, Richard, Francis [GB/GB]; 22 Fox Hollow, Bar Hill, Cambridge CB3 8PK (GB).

(74) Agents: CRAWFORD, Andrew, Birkby et al.; A.A. Thornton & Co., Northumberland House, 303-306 High Holborn, London EC1V 7LE (GB).

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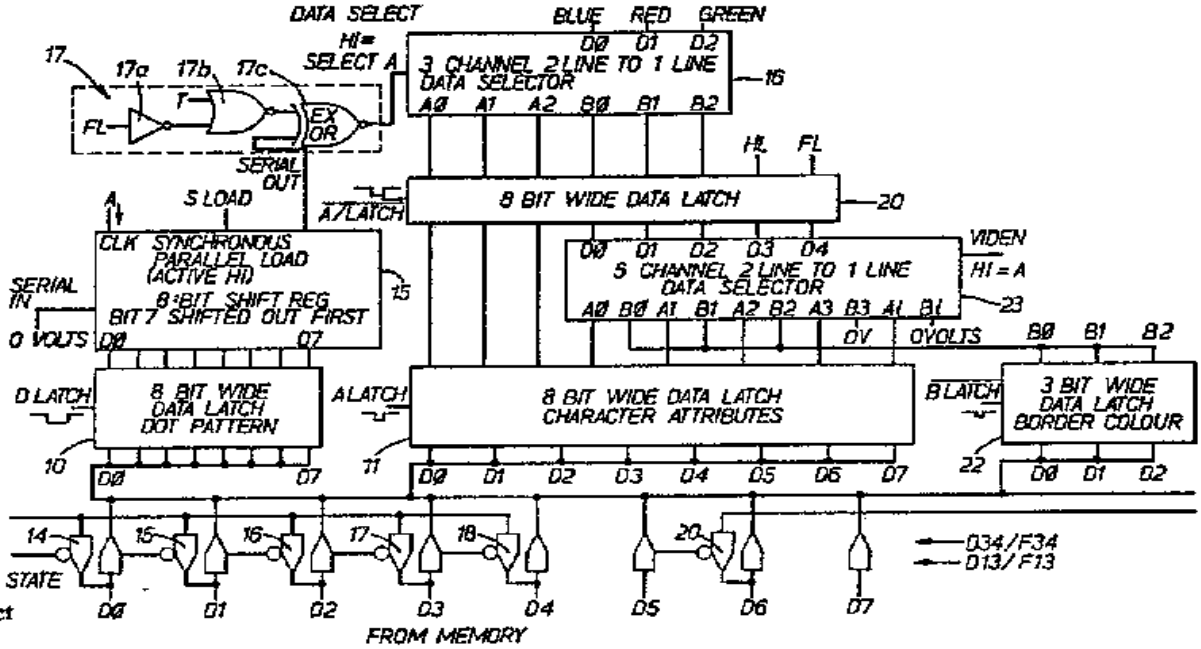

(57) Abstract

A coloured display for a computer is derived using a first set of digital words representing locations in a pixel matrix for the pattern to be displayed and a second set of digital words representing foreground and background colours for the pattern on the basis of a conventional character display whereby to reduce the amount of storage required for the colour information while permitting high resolution graphics. Circuits are provided for converting digital R, G, B signals into analogue Y, U, V signals and each of these circuits comprises a control transistor in whose collector circuit is connected the base of an output transistor and in whose emitter circuit are connected parallel switches and resistances which switches are controlled by signals derived from the digital R, G, B signals whereby to alter the base bias of the output transistor.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 107 687**
B1

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: **06.07.88**

(51) Int. Cl.⁴: **G 09 G 1/28**

(21) Application number: **83901331.5**

(22) Date of filing: **22.04.83**

(86) International application number:
PCT/GB83/00119

(87) International publication number:
WO 83/03916 10.11.83 Gazette 83/26

(54) **DISPLAY FOR A COMPUTER.**

(30) Priority: **22.04.82 GB 8211723**

(43) Date of publication of application:
09.05.84 Bulletin 84/19

(45) Publication of the grant of the patent:
06.07.88 Bulletin 88/27

(84) Designated Contracting States:
AT BE CH DE FR GB LI LU NL SE

(56) References cited:
DE-A-2 940 322
FR-A-2 083 639
US-A-4 303 912

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EP 0 107 687 B1

Courier Press, Leamington Spa, England.